Power Distribution and Decoupling on PCB

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Agenda

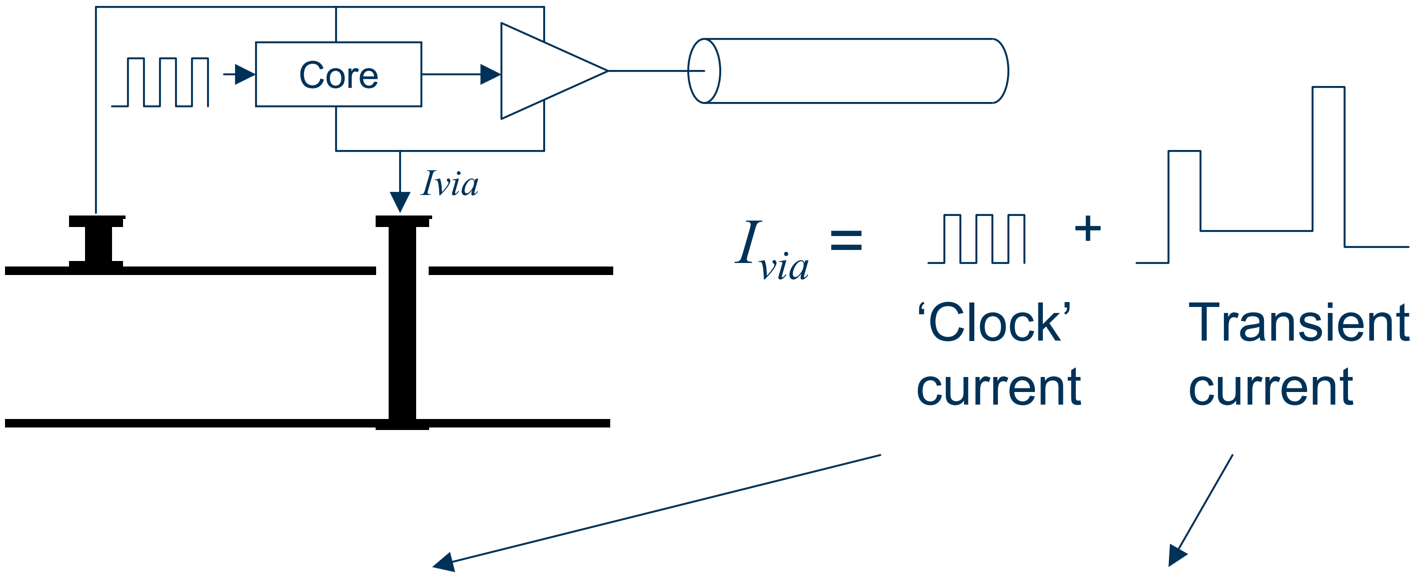
- Transient/periodic sources.
- Transient signals, time domain analyze.
- Demo, time domain simulation.
- Periodic signals, frequency domain analyze.
- Demo, frequency domain simulation.

Trends in power distribution

- Decrease in voltage level, increase in power consumption, faster signal edges.
  - dI/dt increase fast.

  (Example: U -> U/2, P -> 2P, tr -> tr/2 $\Rightarrow$ dI/dt -> 8*dI/dt)
- The number of voltages increase, splitting of power planes.
  - Small areas as power planes.
  - Large distance from source to consumer (risk of long narrow lines)
- Power distribution design will be an increasing critical issue in the future. Old design roles will not work.
- Need of tools to simulate power distribution or get the knowledge how to make a working layout.

Types of current sources



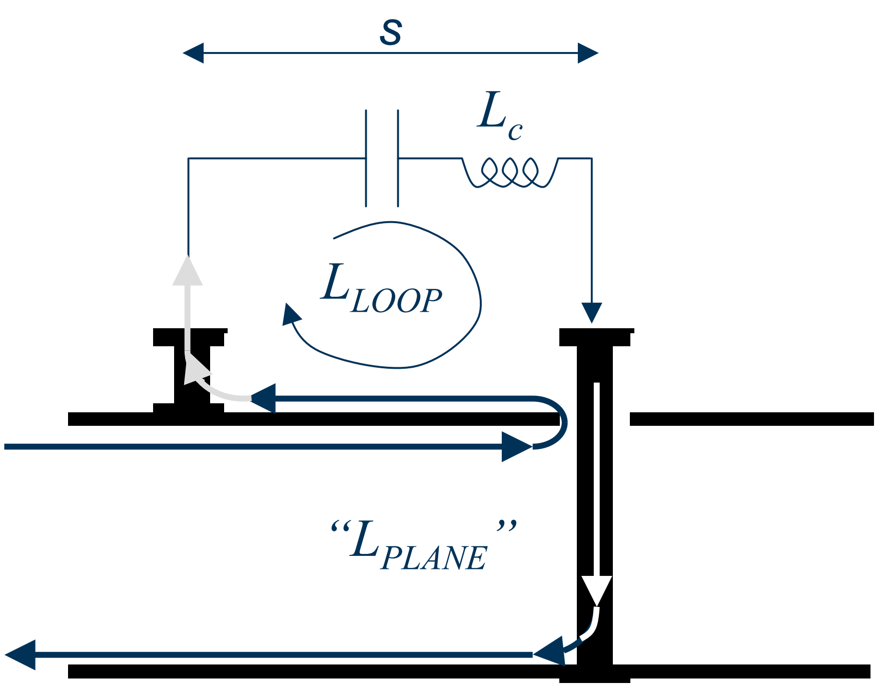
Periodic continuous signal
- Spectra constant in time
- Fundamental frequency
  + harmonics
- Frequency domain analyze

Non periodic signal
- Spectra change during time
- Energy spread over large
  frequency spectrum
- Transient analyze

Non periodic signals, transient signals

- Signal origin from transient changes in signals level or power consumption.
  Examples:
  - Change of logical state of a large bus.
  - Reset -> active state.
  - Power down function of blocks in e.g. processor.
- Signal energy spread over a large continuous frequency range.
- Spectra change in time.
- Resonance circuits not strengthen. Resonance’s from board edges have small influence.
- ‘Short’ time of analyze, only a few reflections needed.
- Time domain representation of signal preferred.

Current flow on PCB and lope inductance



Total inductance

$$L = L_c + L_{LOOP} + (\text{“}L_{PLANE}\text{”})$$

Decap inductance

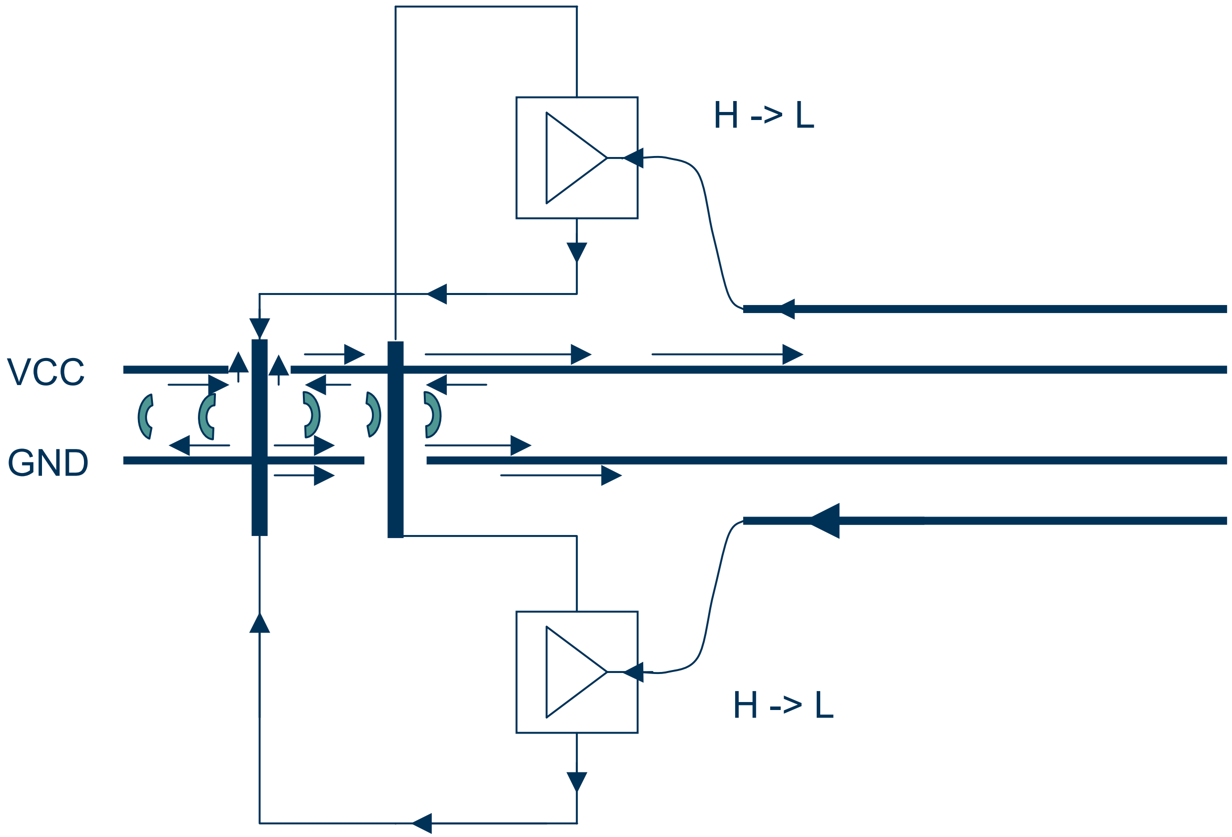
$$L = L_c + L_{LOOP}$$

$$L_{LOOP} = L_{VIA} + L_{trace} + L_{VIA}$$

$$L_{trace} \approx l_{trace} \cdot Z0 \cdot \frac{\sqrt{\varepsilon_r(eff)}}{3 \cdot 10^8}$$

$$L_{VIA} \approx l_{VIA} \cdot \frac{\mu_0}{2\pi} \ln\left(\frac{\frac{s}{2} + \sqrt{\left(\frac{s}{2}\right)^2 - r_{VIA}{}^2}}{r_{VIA}} \right)$$

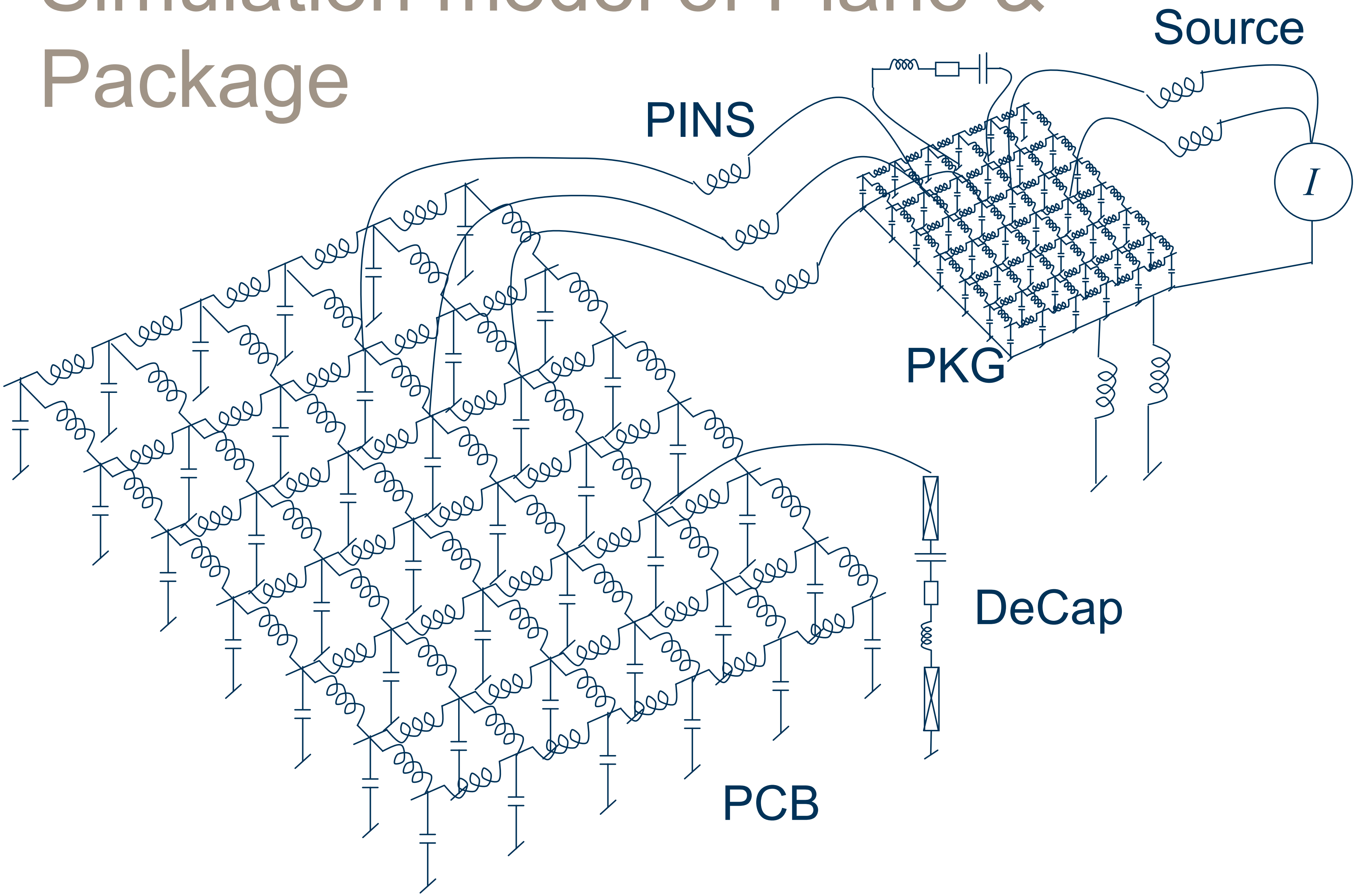
Current injection from circuit and current flow



Simulation tool

- A tool is developed (in MATLAB) to analyze power distribution and decoupling on PCB with a package. The tool support one PCB power distribution plane, decoupling capacitors with traces on PCB, one package, package pins as inductances, one power distribution plane in package with decoupling capacitors within the package.
- Used simulation methods are
  - Time Domain: Modified FTDT
    Use of U, I and C, L instead of E, H and ε, μ
  - Frequency Domain: Modified Nodal Analysis, MNA (SPICE)

Simulation model of Plane & Package



Transient response

- It take time for fields to propagate on PCB (~ 150 mm/ns).
- Low coupling between decoupling capacitors and noise source, low transfer impedance compare to capacitor impedance.
- Decoupling capacitors handle low frequency components only, suffer from inductance.
- Inductance of the decoupling structure set the upper frequency limit of the decoupling capacitor.
- Only planes can handle fast transients.

Example, Allowed inductance in decoupling transient analysis

Allowed voltage ripple ΔU = 50mV

Transient current ΔI = 1A, *tr* = 1ns

No help from planes

$$\Delta U = L \times \frac{dI}{dt} \approx L \times \frac{\Delta I}{tr} \Rightarrow L = \frac{\Delta U \times tr}{\Delta I}$$

$$L = \frac{0.05 \times 1 \cdot 10^{-9}}{1} = 50 \cdot 10^{-12} = 50\,pH$$

Need 20 DeCaps of 1nH inductance to give 50pH

Or 40 DeCaps of 2nH to give 50pH

In a radii of less than 70mm (0.5ns out and 0.5ns back)

Number of decoupling capacitors (if only DeCap handles transients, no helps from planes)

ΔI =1A, t_r =1ns			
Supply Voltage	3% of Vsupp	Nb (L=1nH)	Nb (L=3nH)
3.3	0.1V	10	30
1.2	0.036V	28	84

ΔI =1A, t_r =0.2ns			
Supply Voltage	3% of Vsupp	Nb (L=1nH)	Nb (L=3nH)
3.3	0.1V	50	150
1.2	0.036V	139	417

Current into a decoupling capacitor

- The current derivative into a decoupling capacitor is small

$$U = L \times \frac{dI}{dt} \Rightarrow \frac{dI}{dt} = \frac{U}{L}$$

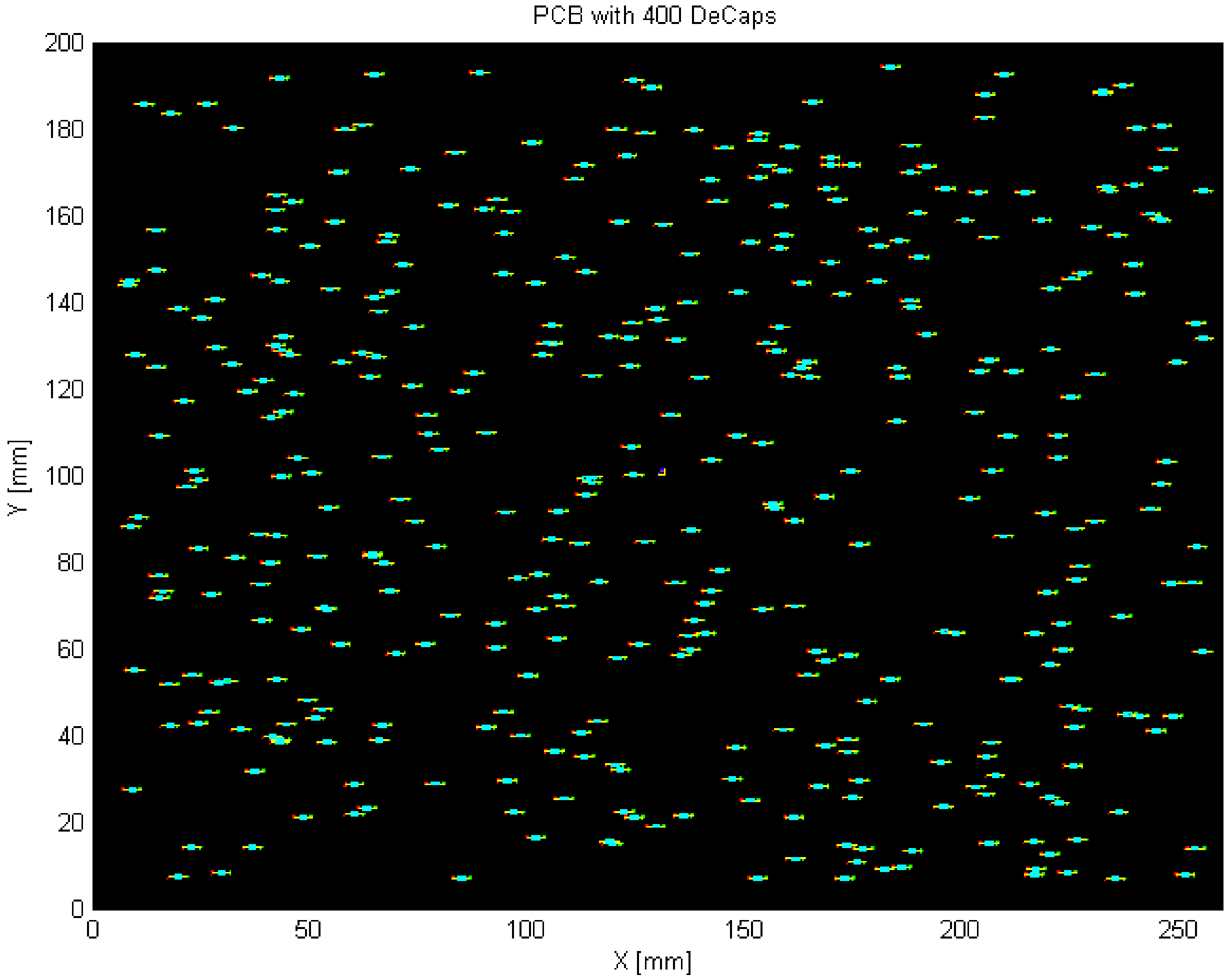
Example;
U = 50 mV,
L = 2 nH

$$\frac{dI}{dt} = \frac{U}{L} = \frac{50 \cdot 10^{-3}}{2 \cdot 10^{-9}} = 25 mA / ns$$

- To handle a switching bus (with no help from the capacitance between planes), with amps in load, a lot of capacitors is needed, probably more than possible to place.
- Need to relay on the capacitance between planes.

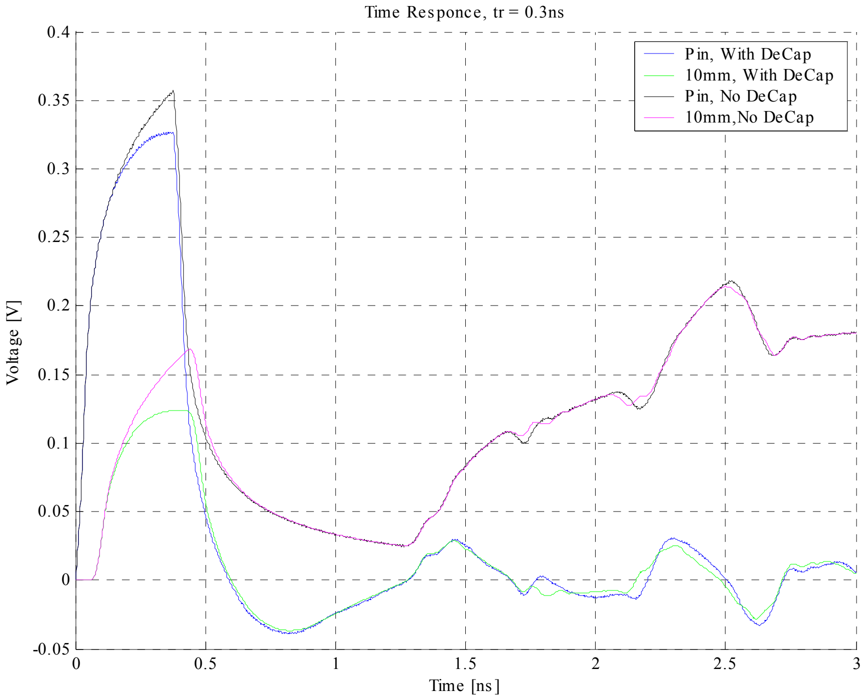
PCB with decoupling used in simulations.

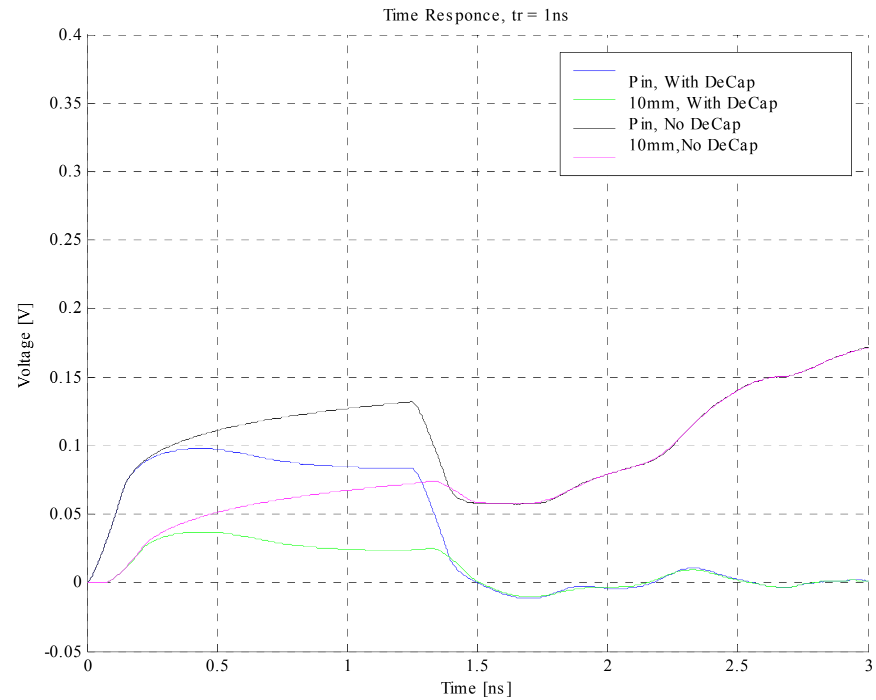
- PCB
  260 x 200 mm,
  FR4
  thickn. d =
  0.13mm
- Up to 400
  Decaps
- Total 2mm
  trace /decap,
  C=100nF
  L=0.85nH
  R=0.01Ohm
- Source in
  center of PCB



Transient voltage noise on PCB, dependent on t_r

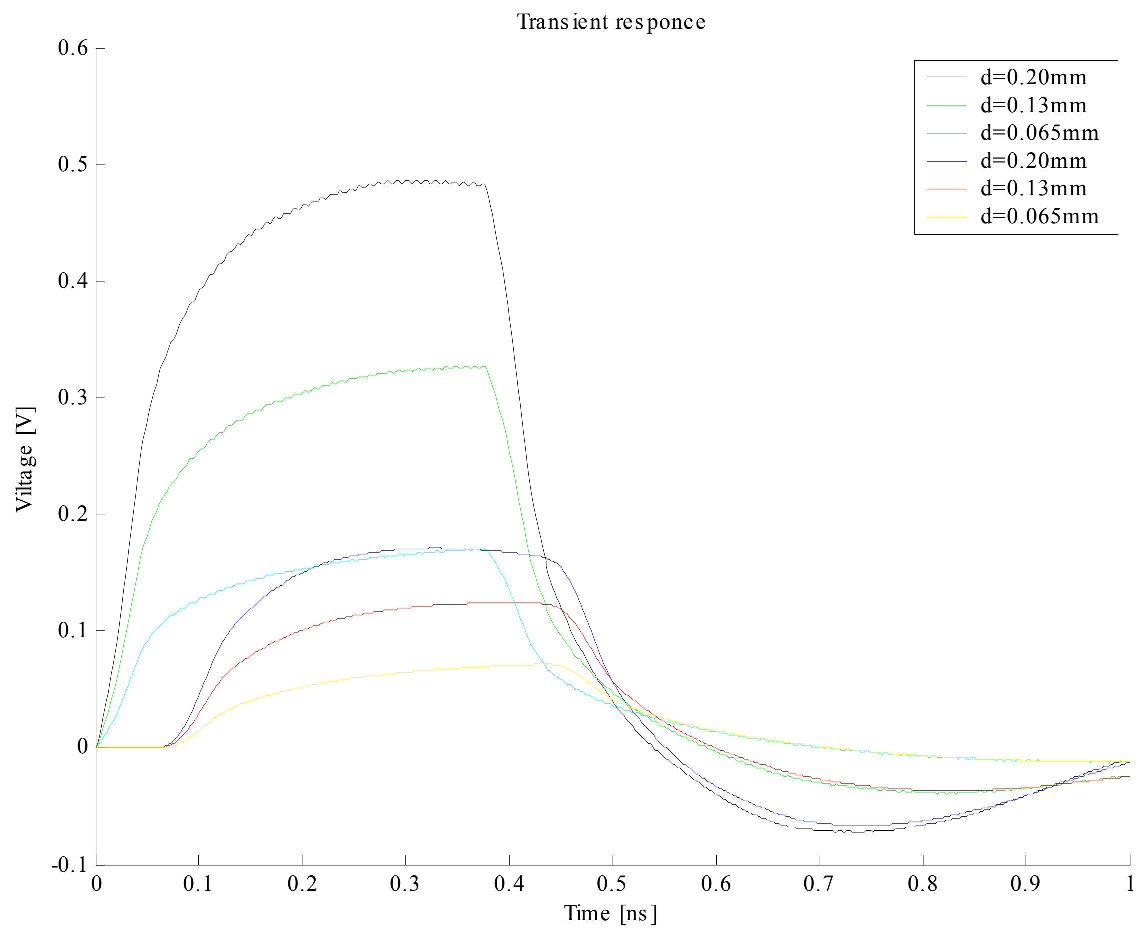
- Source at center of PCB, No DeCap or 400 DeCaps
- tr = 0.3ns or 1.0ns, current = 1A step.





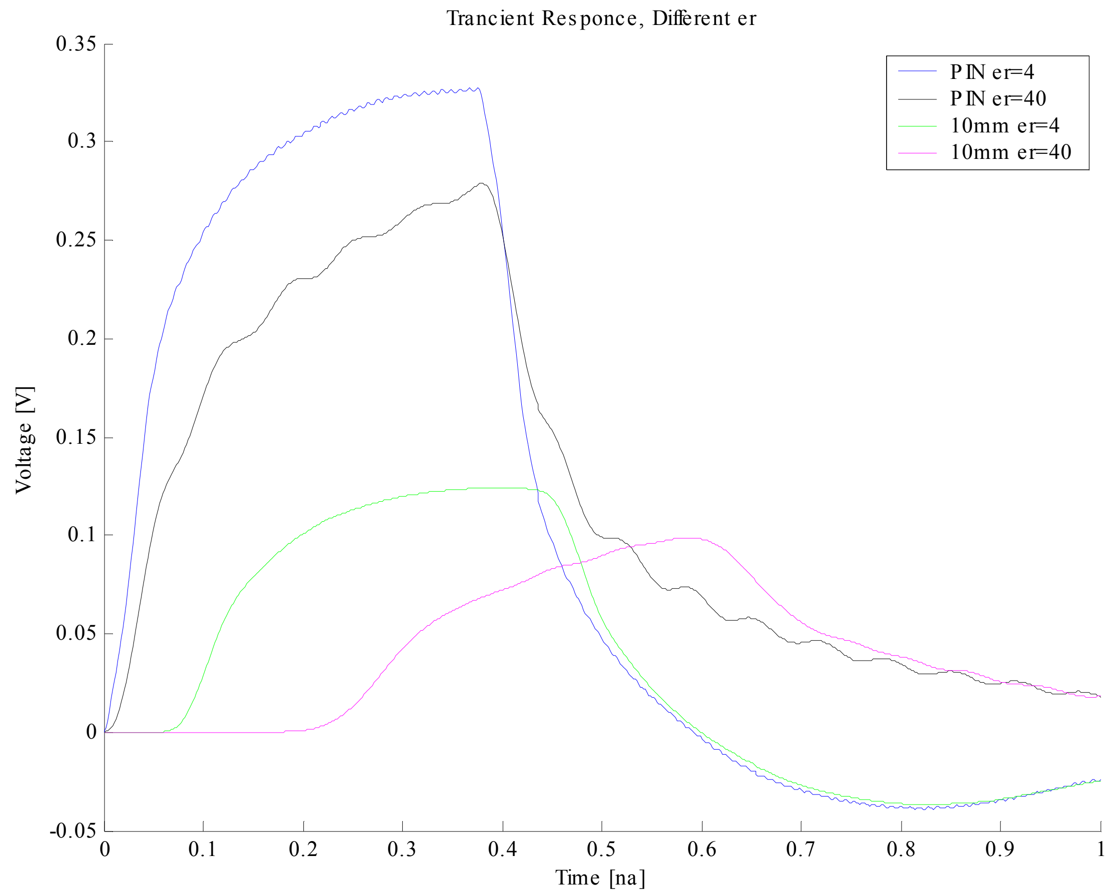
Transient voltage noise on PCB, dependent on plane distance d

- Source at center of PCB, 400 DeCaps
- tr = 0.3ns, current = 1A.
- Plane distance d = 0.20mm, 0.13mm or 0.065mm
- Test points: Center and 10mm from center

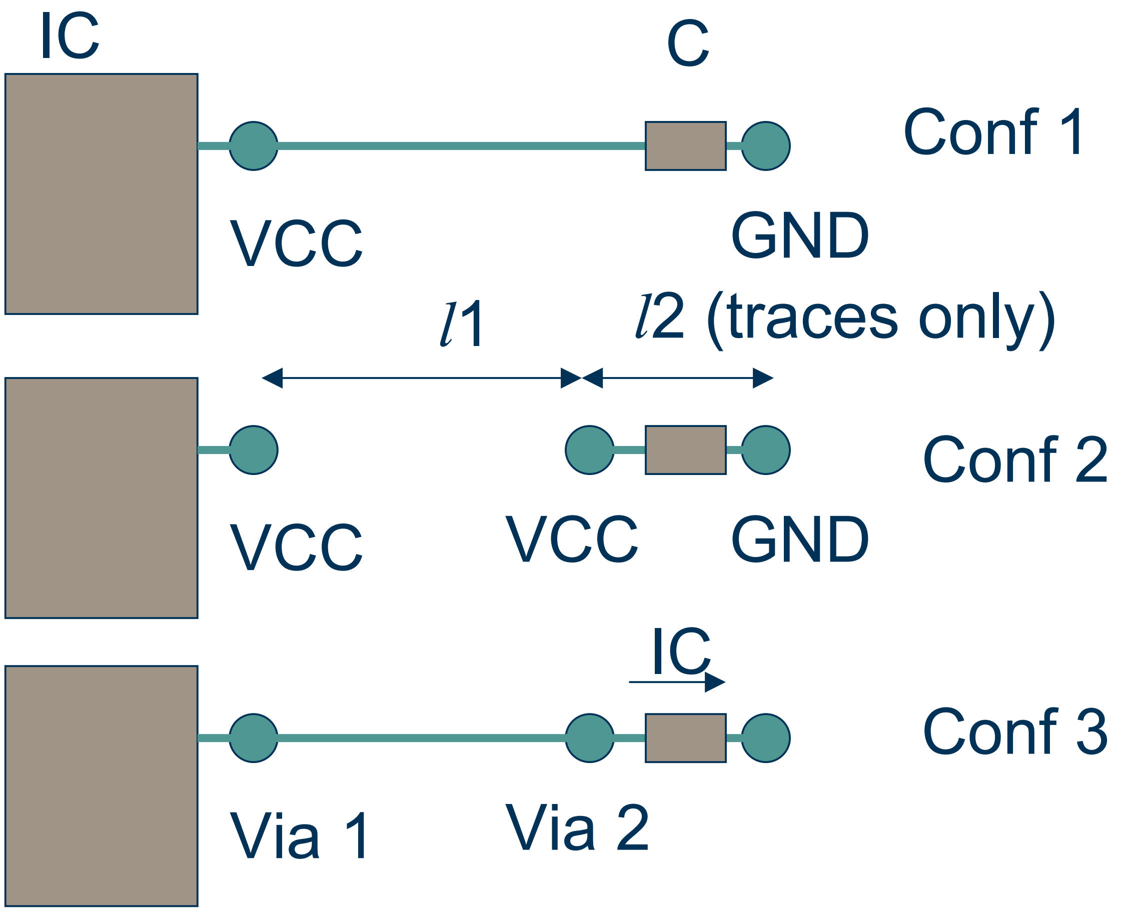


Transient voltage noise on PCB, dependent on ε_r

- Source at center of PCB, 400 DeCaps
- tr = 0.3ns current = 1A.
- ε_r = 4 or 40.



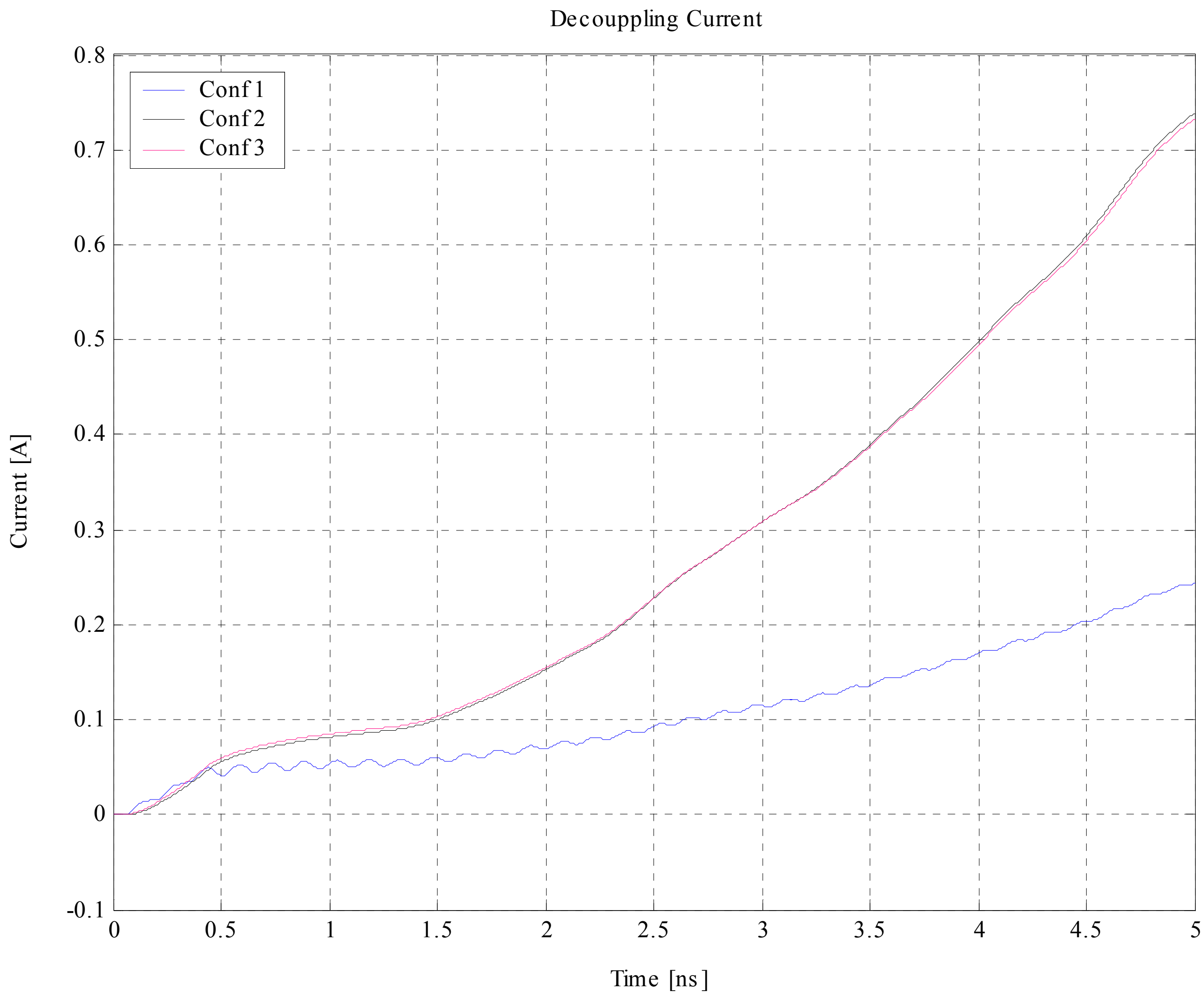
Different methods of connection of DeCaps



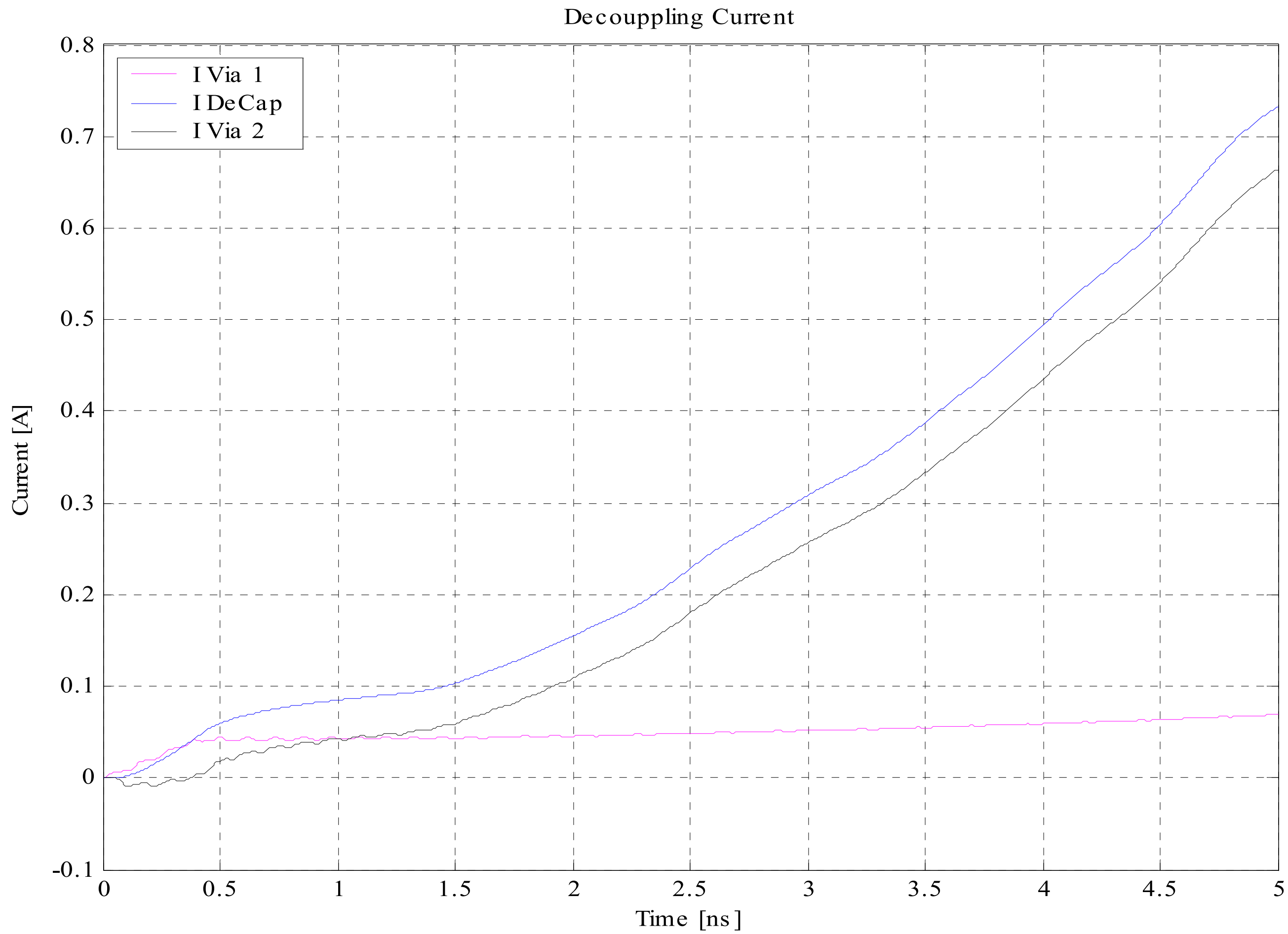
- *l*1 = 10 mm
  *l*2 = 2 mm
- L DeCap = 0.85nH

Current through DeCaps with different configurations

- *l*1 = 10 mm
  *l*2 = 2 mm
- One DeCap on PCB
- L DeCap = 0.85nH
- tr = 0.3ns



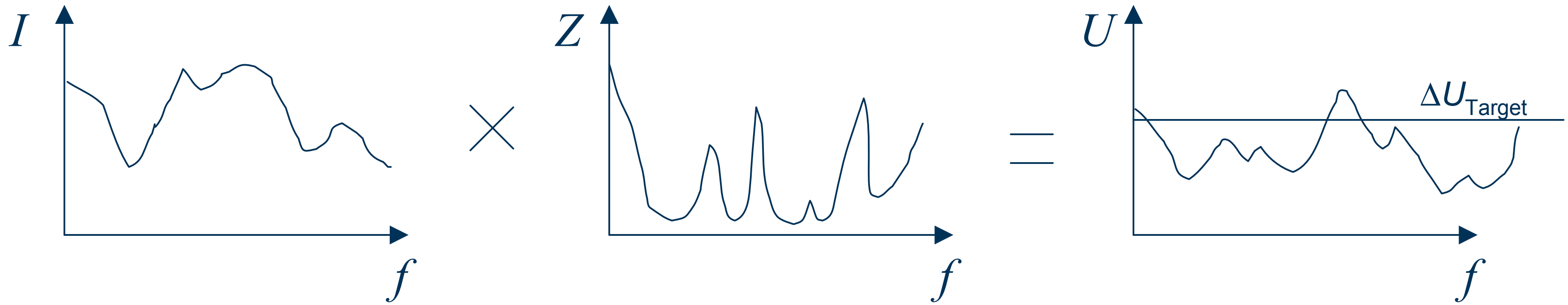
Current in vias and decoupling capacitor, configuration 3



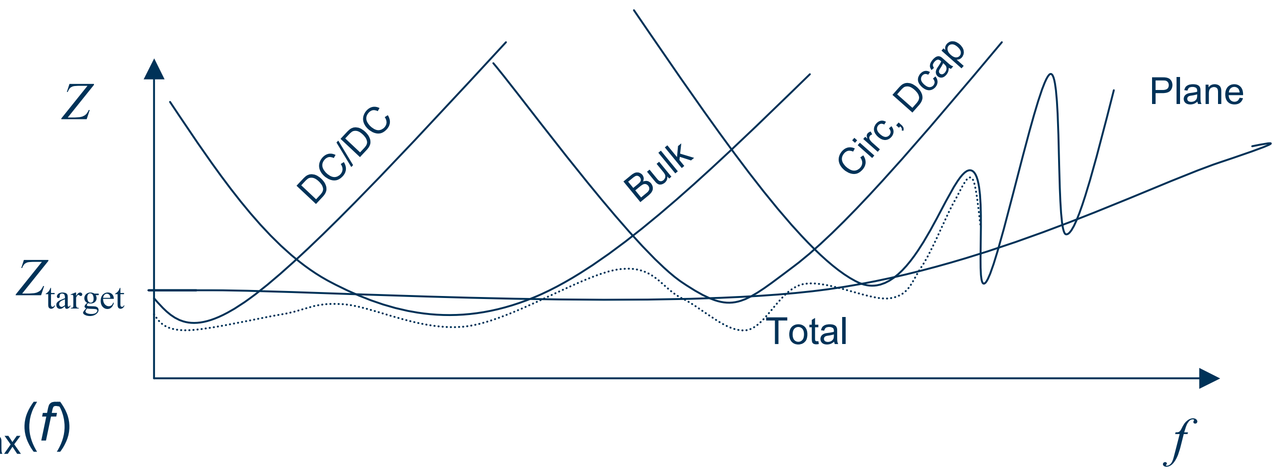
Periodic, continuous signal

- Signals origin from clocks, periodic in time.
- Clock signal can be represented as a fundamental sinusoidal frequency and its harmonics.
- Resonance's strengthen.
- Need long time to reach steady state (*Q*-factor dependent).
- Distant objects affect resonance's, as board edges.
- Frequency domain analyze preferred.

Impedance requirement (frequency domain)



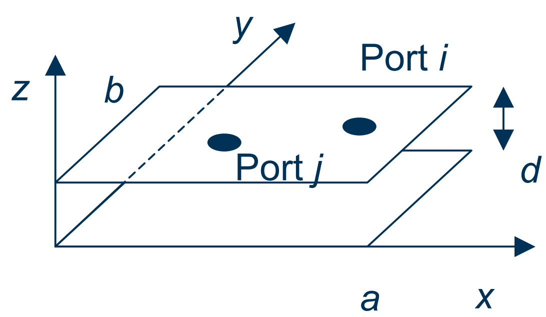
One design method; Maximum noise voltage over frequency



$Z_{target}(f) = \Delta U_{Target} / I_{max}(f)$

Resonance's in power planes, Impedance(*f*)

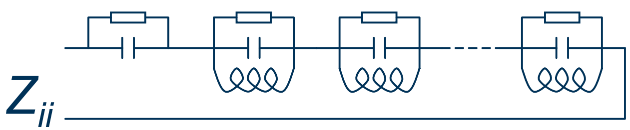
- Impedance in parallel planes is caused by cavity resonance given by the conductive planes and board edges



$$\nabla \times \overline{E} = -\frac{\partial \overline{B}}{\partial t} \qquad \nabla \times \overline{H} = \bar{i} + \frac{\partial \overline{D}}{\partial t}$$

Boundary Condition, Green's function

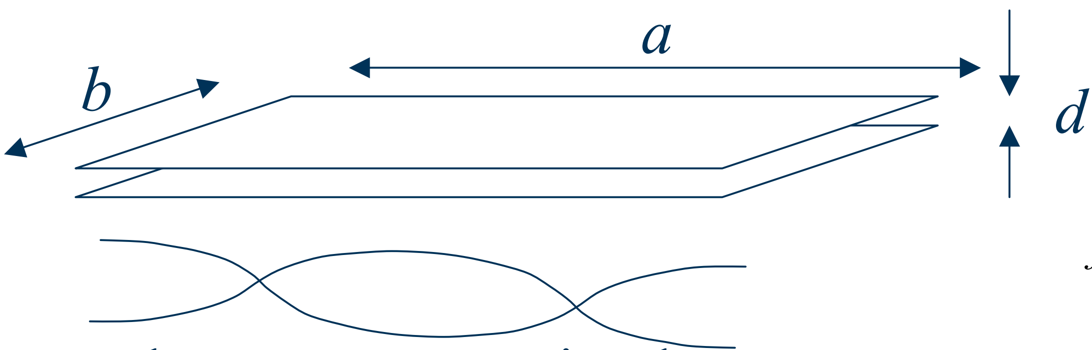
$$U_i = Z_{ij} \times I_j$$



$$Z_{ij} = j\omega\mu d \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{\varepsilon_{mn}}{(k_{mn}^2 - k^2)} f(x_i, y_i, x_j, y_j)$$

$$Z_{ij} = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \frac{N_{mni} N_{mnj}}{j\omega C_{mn} + 1/j\omega L_{mn} + G_{mn}} f(x_i, y_i, x_j, y_j)$$

PCB board, planar structure.



Voltage resonance in planes

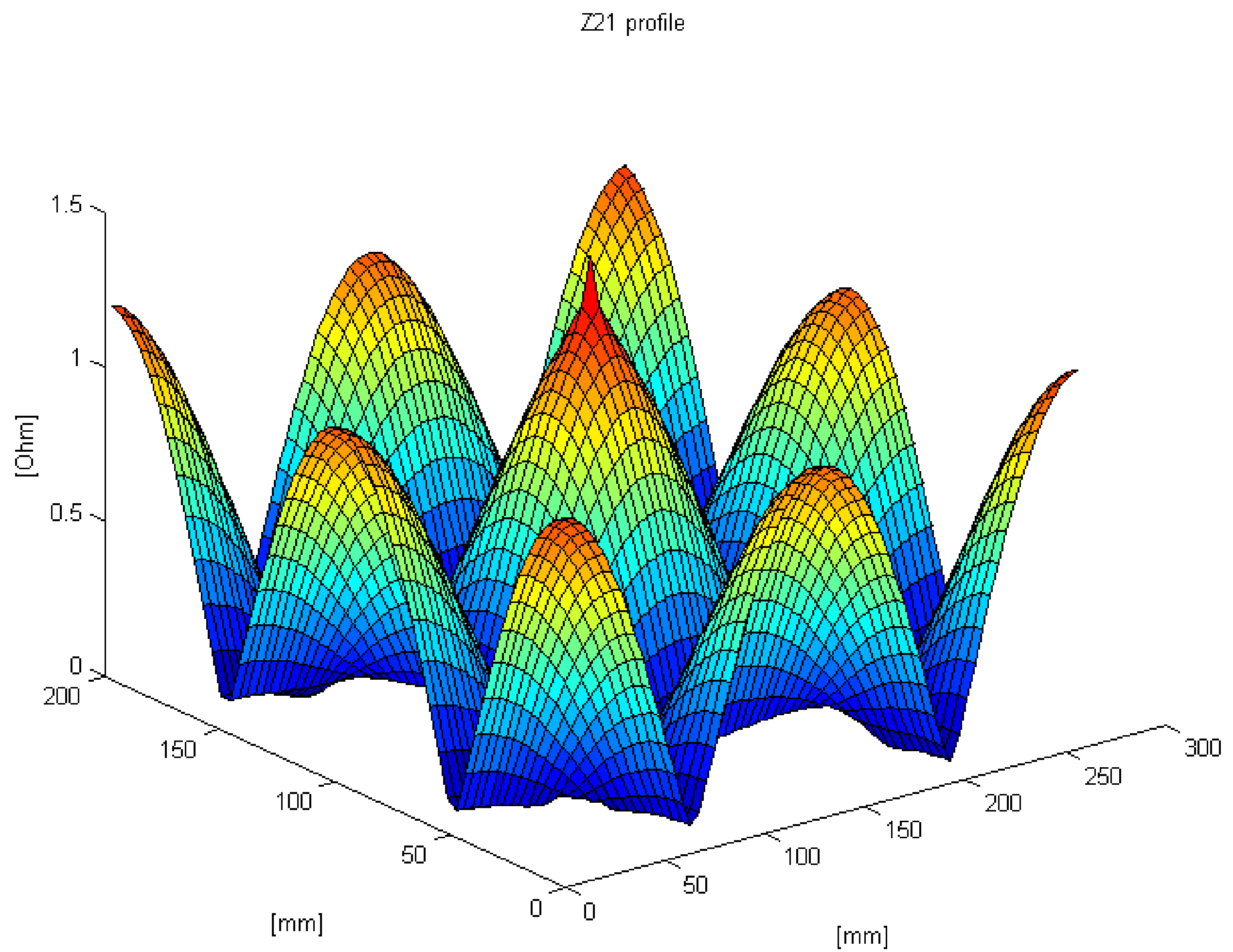
$$f_{r,mn} = \frac{c}{2\sqrt{\varepsilon_r}} \sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2}$$

Possible resonance frequencies for a PCB with *a* = 265 mm *b* = 175 mm. ε_r=4.5 (*m* = 0 to 3, *n* = 0 to 3)
Port position dependent.

E.g. source in the centre of PCB will only have even values of *m* and *n*

Resonance frequency [MHz]				
*m**n*	0	1	2	3
0	-	402	804	1205
1	266	482	846	1234
2	532	666	964	1317
3	798	893	1132	1445

Example of resonances on PCB



Input impedance of PCB with decoupling. Frequency domain

- PCB
  260 x 200 mm,
  FR4
  thickn. d =
  0.13mm
- Up to 400
  Decaps
- Total 2mm
  trace /decap,
  C=100nF
  L=0.85nH
  R=0.01Ohm
- Source in
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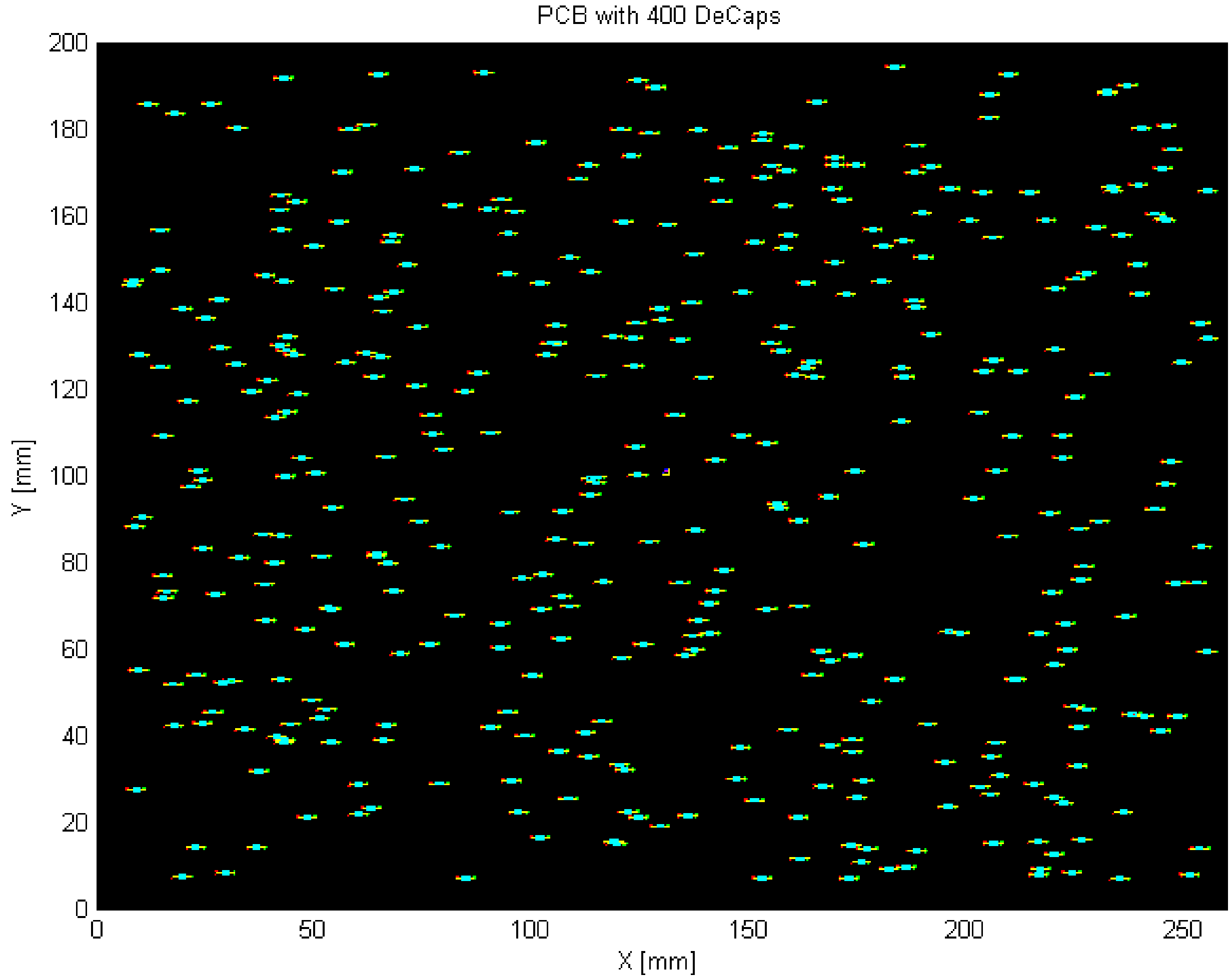
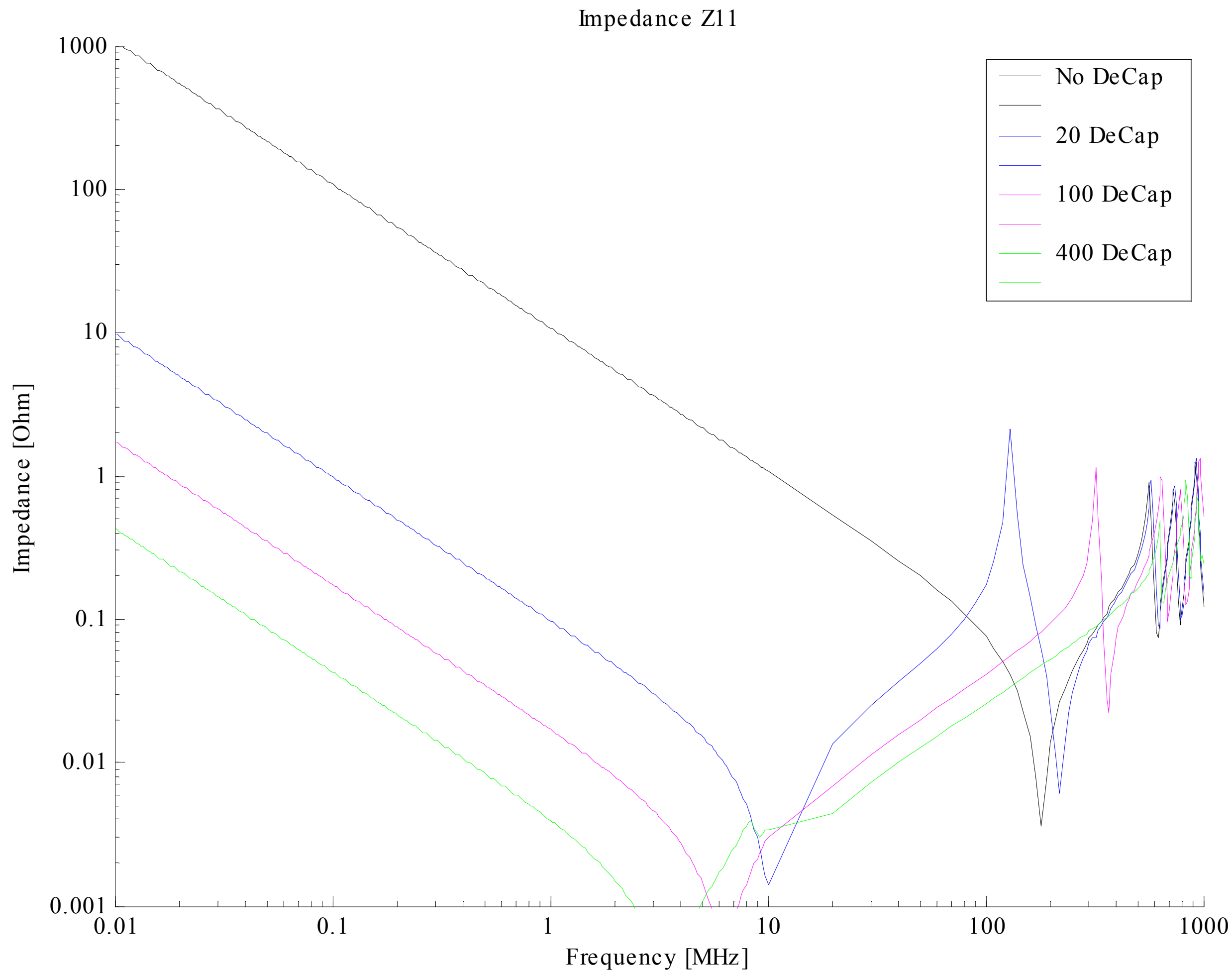


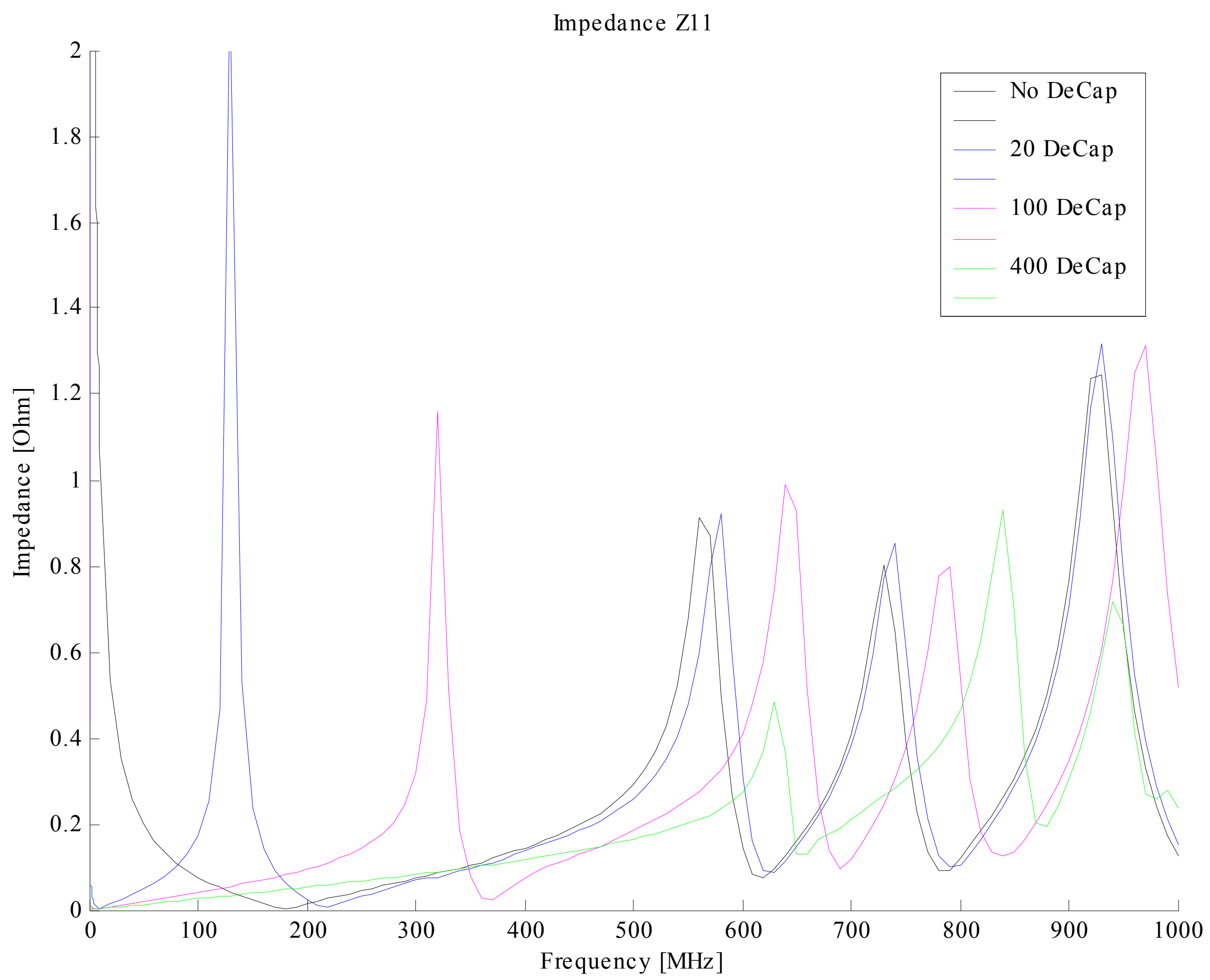
Input Impedance Z11 of PCB with diff. number of DeCaps

- PCB with diff. number of DeCaps
- Below 100MHz the amount of capacitance sets the impedance, noise level.

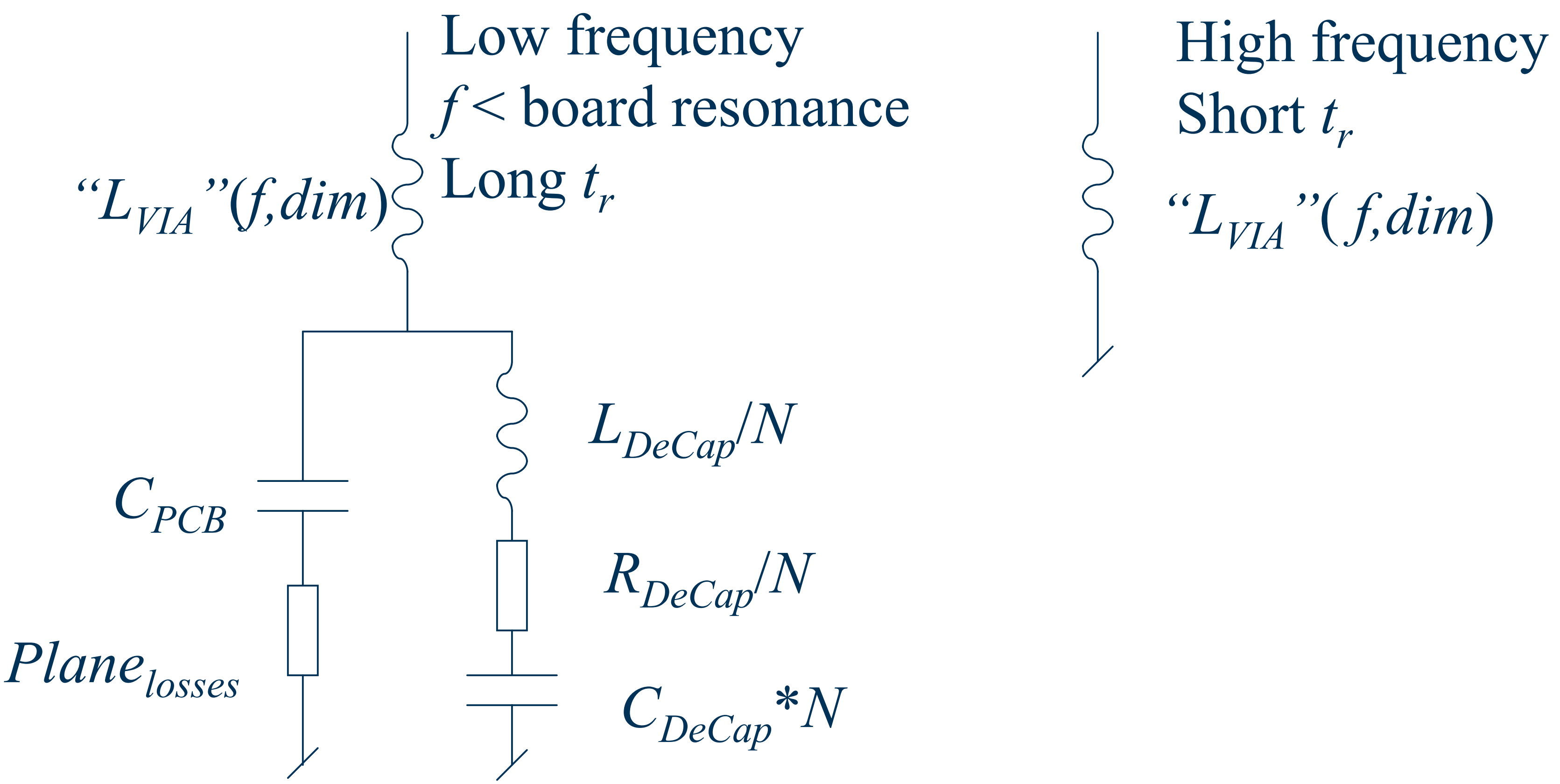


Input Impedance Z11, cont

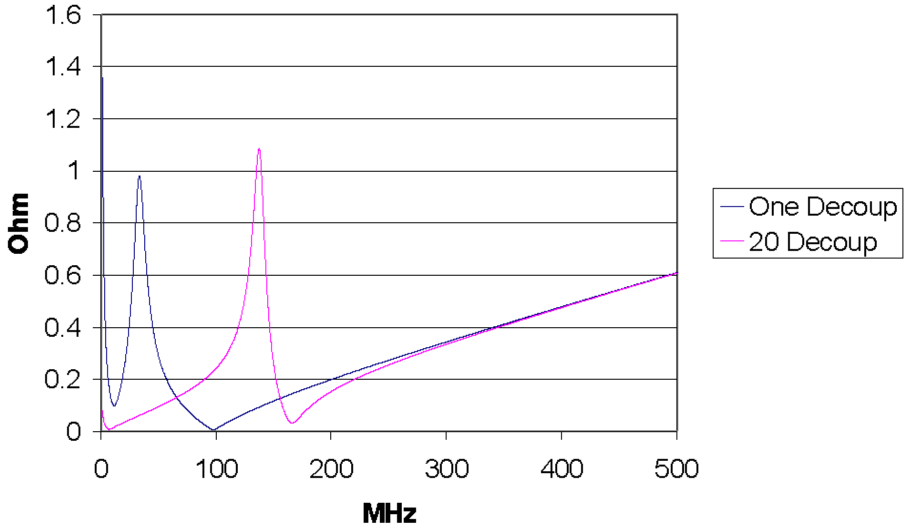
- Resonances due to De-Caps can be observed, (first resonance peak).
- Above 500, 600 MHz De-Caps make no difference on impedance amplitude at resonance.



Lumped model of power distribution on PCB



Impedance of the lumped model at low frequency

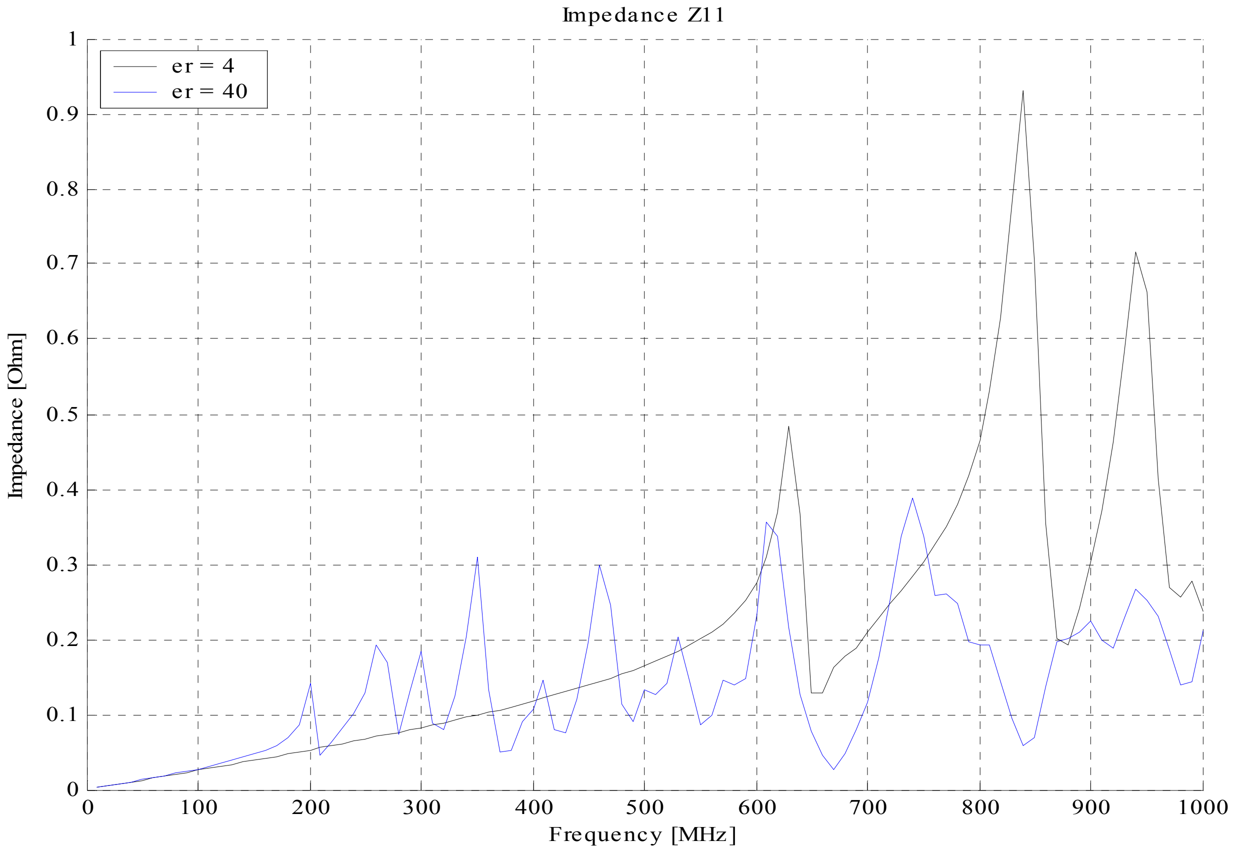


$$\omega_p \approx \frac{1}{\sqrt{C_{PCB} \cdot \frac{L_{DeCap}}{N}}}$$

$$Z_p \approx \frac{L_{DeCap}}{R_{DeCap} \cdot C_{PCB}}$$

Influence of high ε_r material

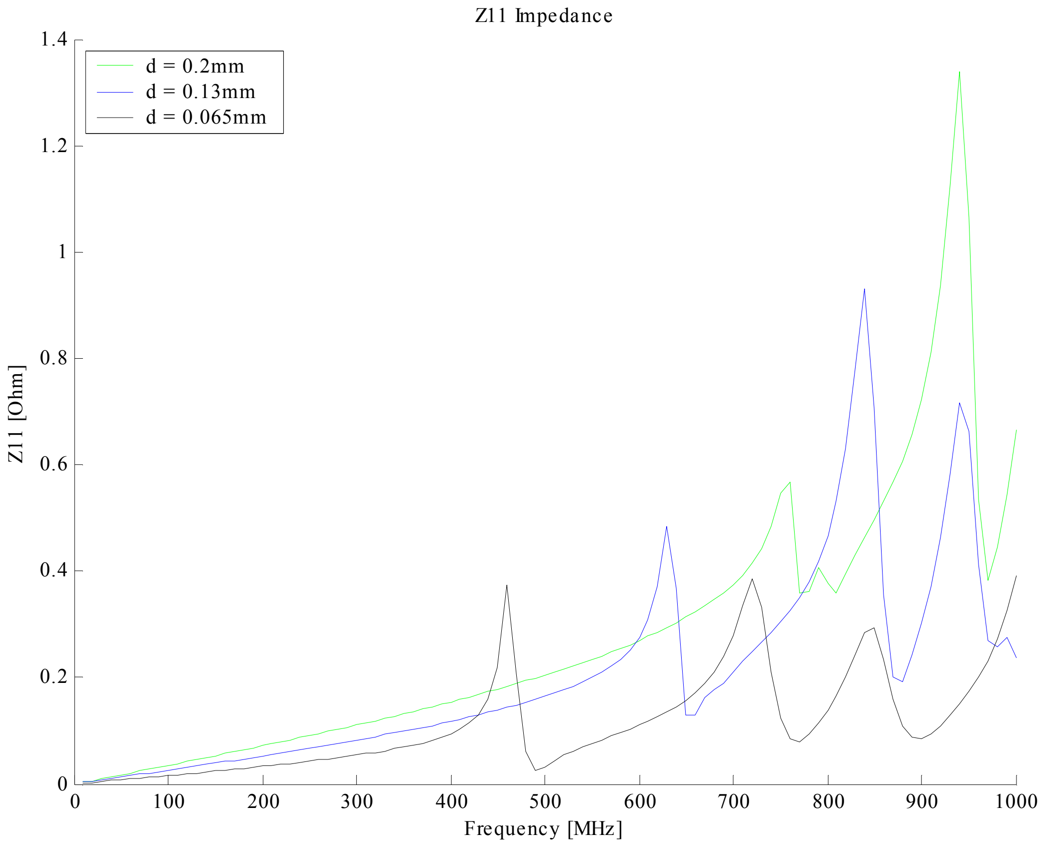
- PCB with 400 DeCaps
- d = 0.13mm
- ε_r = 4 and 40



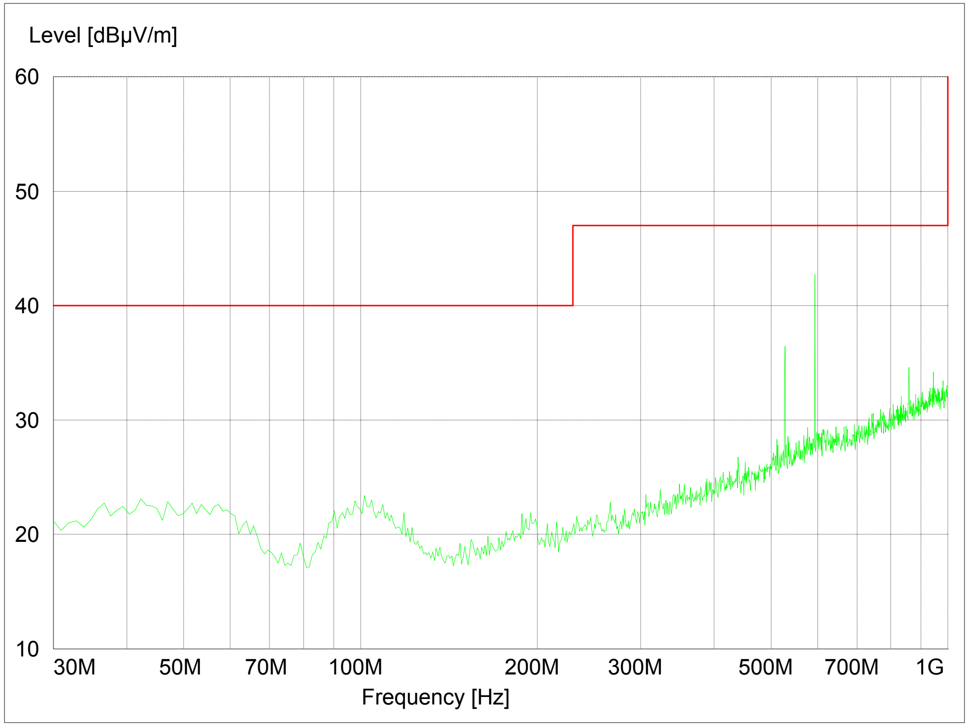
Plane distance influence on impedance

- PCB with 400 DeCaps
- d = 0.065mm
  0.13mm
  and 0.2mm
- $\varepsilon_r = 4$

- A Thin distance between plane gives a lower impedance

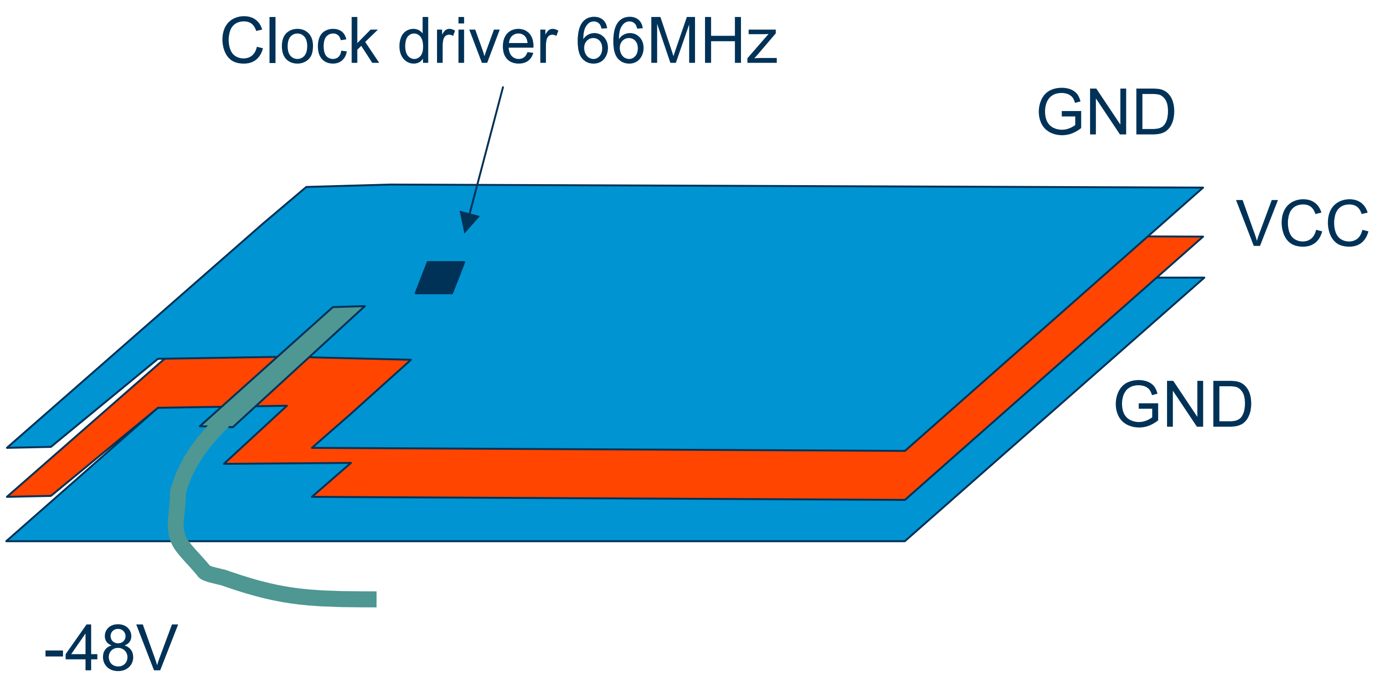


Radiated emission from PCB with EMI problem.

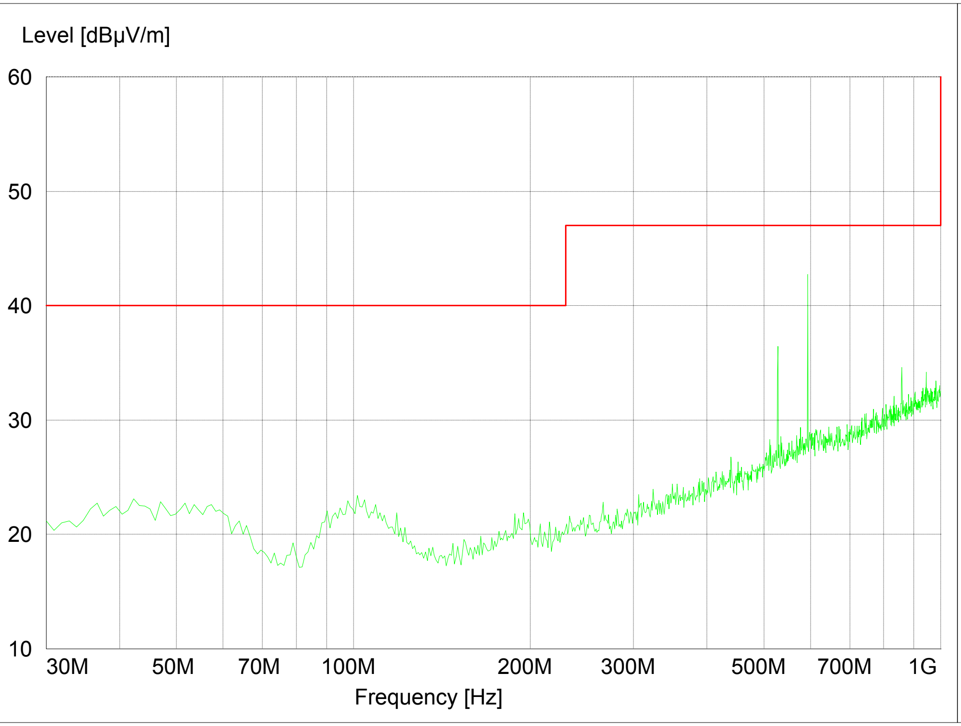


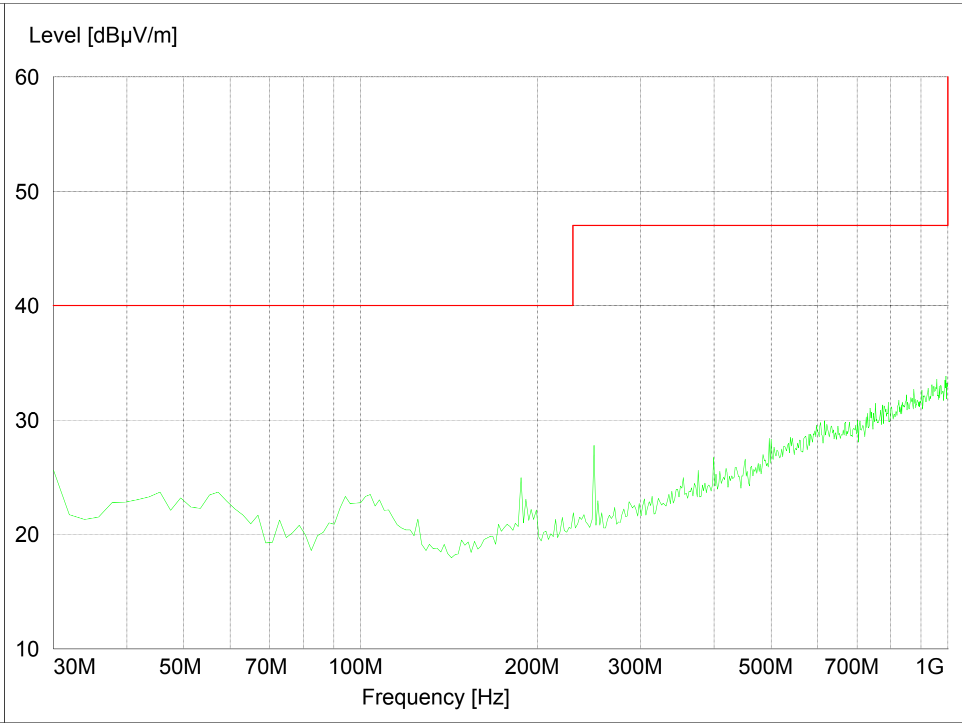
Before modification

PCB plane profile and stack-up of a PCB with EMI problem.



Radiated emission of a PCB with EMI problem.





Before modification

After modification, remove of voltage plane below –48V trace

Conclusion

- Decoupling capacitors is needed. The more the better.
- Decoupling capacitors handle low frequency noise only
- Planes alone have to handle high di/dt noise
- Impedance $Z \propto d$ (plane separation) $\Rightarrow$ Noise $\propto d$.
- Decoupling placement dependent on PCB stuckup
  - 2-layer board: Trace length between circuit and DeCap is critical.
  - PCB with large distance between planes, e.g. 4-layers board: DeCaps need to be placed near circuits.
  - PCB with small distance between planes ($d<0.15$mm): Placement of decoupling capacitor is not critical (place were it is convenient).
- Inductance sets the limit in frequency of the decoupling. Beware or trace inductance.
- High ε material have low effect on noise.
- Needed capacitance on PCB is set by needed “charge backup”

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